PAC900S12-B2 PSU

Technical Manual

Issue 1.0

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About This Document

Purpose

This document describes the PAC900S12-B2 power supply unit (PSU), including its features, electrical specifications, applications, and communication.

The figures provided in this document are for reference only.

Intended Audience

This document is intended for:

- Hardware engineers
- Software engineers
- System engineers
- Technical support engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazard with a medium level of risk which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazard with a low level of risk which, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.
NOTE	Supplements the important information in the main text. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Changes between document issues are cumulative. The latest document issue contains all updates made in previous issues.

Issue 1.0 (2020-06-30)

This issue is the first official release.

Contents

1 Product Overview

The PAC900S12-B2 supports AC input of 90 V to 264 V and HVDC input of 180 V to 300 V. The PSU provides one output and supports three output modes MV12, SV12 and MV6. The rated output power is 900 W. The PSU is hot-swappable, equalizes current, and supports 1+1 or 2+2 parallel connection. The PSU supports PMBus communication, and sends the PSU information to the system to facilitate monitoring and management.

Model Naming Convention

P	AC	900	S	12	_	B	2
1	2	3	4	5		6	7

1 — Embedded power

2 — AC input

3 — Output power: 900 W

4 — Single output

5 — Output voltage: 12 V DC

6 — 80 Plus platinum energy efficiency certification

7 — Serial number

Features

- Efficiency: 94% (V_{in} = 230 V AC, P_{out} = 450 W, T_A = 25°C, without a fan)
- Depth x Width x Height: 183.0 mm x 68.0 mm x 40.5 mm
- Power grid: 110 V AC/220 V AC single-phase, 240 V DC
- Supports AC input protection for undervoltage, overvoltage, overcurrent, short circuit, and PFC overvoltage
- Supports HVDC input protection for overvoltage, undervoltage, and PFC overvoltage
- Supports output protection for overvoltage, overcurrent, short circuit, and overtemperature
- I2C for control, programming, and monitoring
- CE, NRTL, TUV, CCC, BSMI, BIS certification and CB report available
- 80 Plus platinum energy efficiency certification
- IEC 60950-1, EN 60950-1, UL 60950-1, GB 4943.1, IEC 62368-1
- RoHS compliant

Applications

Servers

2 Features

2.1 Environmental Specifications

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Operating temperature (T_A)	5	25	55	°C	The PSU is able to start at –10°C, but there are no requirements on the PSU performance. When the temperature ranges from 55°C to 65°C, the PSU can run reliably at half load for a long period of time.
Storage temperature	–40	25	85	°C	-
Relative humidity	5	-	95	% RH	Non-condensing. The PSU can work properly.
Altitude	–60	0	5000	m	5000 m in CCC certification. When the PSU is not working, it can be placed at an altitude of 15,000 m.
Atmospheric pressure	61	-	106	kPa	The PSU meets the atmospheric pressure at an altitude of 4000 m.
Low atmospheric pressure	-	-	4000	-	Low atmospheric pressure test at an altitude of 4000 m and with rated input of 230 V AC. When the altitude ranges from 1800 m to 4000 m, high-temperature derating applies and the temperature decreases by 1°C for each additional 220 m.

2.2 Input Specifications

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
AC input voltage	90	-	264	V	-
Rated AC input voltage	100	220	240	V	-
HVDC input voltage	180	240	300	V	The PSU operation should not be affected if the L and N ports of the PSU and the input positive and negative terminals are reversely connected
AC input frequency	47	50/60	63	Hz	-
THDi (MV12 output mode)	-	-	-	%	T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz), no requirement when load is < 10% load
	-	-	20		T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz), 10% load
	-	-	10		T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz), 20% load
	-	-	5		T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz), ≥ 30% load
THDv	-	-	10	%	THDv ≤ 10%: The PSU can work properly
Power factor (MV12)	0.94	-	-	-	T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz) or 240 V AC (60 Hz), 10% load
	0.96	-	-	-	T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz) or 240 V AC (60 Hz), 20% load
	0.98	-	-	-	T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz) or 240 V AC (60 Hz), 50% load
	0.99	-	-	-	T_A = 25°C, V_{in} = 208 V AC (60 Hz) or 230 V AC (50 Hz) or 240 V AC (60 Hz), 100% load
Maximum AC input current (RMS)	-	-	11	A	V_{in} = 100 V AC, full load

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Maximum HVDC input current (RMS)	-	-	5	A	V_{in} = 240 V DC, full load
AC input DC bias	-	-	50	mA	Rated input, full load range (take the average value of the parallel test)
Input inrush current	-	-	30	A	ETSI300132-3 compliant
AC input system	-	Single-phase three-wire input	-	-	Supports 110 V AC/220 V AC single-phase input and dual-live-wire input.
Standby power	-	-	1	W	T_A = 25°C, V_{in} = 115 V AC/230 V AC/240 V DC. The fan is shut down. The output is shut down. The PSU works in deep sleep mode.
	-	-	5		T_A = 25°C, V_{in} = 115 V AC/230 V AC/240 V DC. The fan works at the lowest rotational speed, and the output is 0 A. The standby PSU works in cold standby mode.
Harmonic current	-	-	-	-	Meets the test requirements of class A equipment (T_A = 25°C).
Input overcurrent or short circuit protection	-	-	-	-	If an internal fault occurs in the PSU, the upstream C32 circuit breaker is not allowed to trip.

NOTE

- The PSU can withstand an input voltage of 318 V AC for 48 hours (non-working state is acceptable).
- The inrush current should meet the requirements in ETSI EN 300 132-3.
- When testing the maximum input current, ensure that the voltage of the power input port meets the requirement and that the output is 900 W.

2.3 Output Specifications

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Number of outputs	-	-	-	1	-	There is one output. The output mode can be MV12, SV12 and MV6. PSON12V# at high level: MV6 output mode PSON12V# at low level: MV12 output mode. • When the PSON12V# signal is at low level, the following working states are presented by the IP PRESENT#: 1. IP PRESENT# at high level, MV12 output mode. 2. IP PRESENT# at low level: SV12 output mode. The power indicator blinks green at 1 Hz. 3. IP PRESENT# detection validity time ≥ 25 ms, switching delay ≤ 200 ms (including the detection time)
Output power	MV12	-	-	900	W	V_{in} = 90–264 V AC or 180–300 V DC
	MV6	-	-	60		V_{in} = 90–264 V AC or 180–300 V DC
Output voltage setpoint	MV12/ SV12	12.27	12.30	12.33	V	TA = 25°C, rated input (230 V AC, 240 V DC), I_{out} = 3 A.
	MV6	7.30	7.60	7.90		
Output voltage	MV12/ SV12	11.7	12.3	12.6	V	From no load to full load; area I.
	MV6	6.4	7.6	8.2		
Output current	MV12	3	-	75	A	V_{in} = 90–264 V AC or 180–300 V DC, maximum power ≤ 900 W
	MV6	1	-	10		-
	SV12	1	-	45		-

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Energy efficiency certification	-	-	-	-	Platinum	The 80 Plus platinum energy efficiency certification is required.
Source regulation rate	-	–1	-	1	%	-
Output ripple and noise (peak to peak)	MV12	-	-	120	mV	Before the test, add a minimum capacitive load of 540 µF and a minimum load of 3 A at the output end, connect a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor in parallel to the ripple probe, and set the oscilloscope bandwidth to 20 MHz. Put the ripple probe behind the minimum capacitive load.
	SV12	-	-	360	mV	Add a minimum capacitive load of 270 µF and a minimum load of 1 A, connect a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor in parallel to the ripple probe, and set the oscilloscope bandwidth to 20 MHz.
	MV6	-	-	360	mV	Add a minimum capacitive load of 270 µF and a minimum load of 1 A, connect a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor in parallel to the ripple probe, and set the oscilloscope bandwidth to 20 MHz.
Dynamic overshoot amplitude	MV12	11.6	-	12.6	V	Current change rate: 0.5 A/µs, T = 10 ms; load: 25%–50%–25%; 50%–75%–50% Tested with the minimum capacitive load 540 µF.
		11.4	-	12.8	V	Current change rate: 0.5 A/µs, T = 10 ms; load: 50%–100%–50% Tested with the minimum capacitive load 540 µF.

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
	MV6	6.0	-	8.2	V	Current change rate: 0.5 A/μs, T = 10 ms; load: 5%–100% Tested with the minimum capacitive load 270 μF.
	SV12	11.4	-	12.6	V	Current change rate: 0.5 A/μs, T = 10 ms; load: 25%–50%–25%; 50%–75%–50% Tested with the minimum capacitive load 540 μF.
Transient impact power overshoot	MV12	11.4	-	12.8	V	Current change rate: 0.5 A/μs, pulse period 1s–10 ms–1s; load: 65%–130%–65% Tested with the minimum capacitive load.
Overshoot at turn-on	MV12	–5	-	5	%	-
Temperature coefficient	-	–0.02	-	0.02	%/°C	Rated output voltage, rated output current and full range of T_A.
Current share imbalance	MV12	–5	-	5	%	50%–100% load (rated load of a single PSU in parallel mode).
	MV12	–10	-	10	%	200 W–50% load (rated load of a single PSU in parallel mode).
	MV12	-	-	-	%	It is not required when the load is less than 200 W.
Current sharing bus voltage	MV12	5.7	6.0	6.3	V	$I_{MON} = \frac{6}{75} \times I_{out}$ I_{MON}: current sharing bus voltage (unit: V) I_{out}: output current (unit: A) 6/75: coefficient of proportionality
External capacitance	MV12	540	-	22000	μF	-
	SV12	270	-	1000	μF	
	MV6	270	-	1000	μF	

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Hot swap	MV12	11.4	-	12.6	V	The backplane voltage cannot exceed the dynamic requirements for the PSU during the swap. In the MV12 mode, the bus voltage must be greater than or equal to 11.4 V (not applicable when the hot swap is complete within 100 µs). 1. Hot swap does not need to be tested in the case of the removal of a PSU with power on. 2. In a parallel system with the 12 V output, test the PSU with the minimum capacitive load.
	MV6	6.0	-	8.2	V	

NOTE

1. In the isolation process of output overvoltage protection failure during parallel testing, the 12 V bus voltage cannot be lower than 11.4 V.
2. Use active current sharing.
3. 1+1 parallel system: When the total load is less than or equal to the rated load of a single PSU, the current sharing formula is $[I - (I_1 + I_2)/2]/(I_1 + I_2) \times 100\%$;

   When the total load is greater than the rated load of a single PSU, the current sharing formula is

   $[I - (I_1 + I_2)/2]/IN \times 100\%$.
4. In a 2+2 parallel system, the current sharing formula is as follows on the premise that the 1+1 current sharing requirements are met:

   $\text{Max}[\text{Max}(I, I_2, I_3, I_4) - \text{Ave}(I_1, I_2, I_3, I_4), \text{Ave}(I_1, I_2, I_3, I_4) - \text{Min}(I_1, I_2, I_3, I_4)]/IN \times 100\%$.

2.4 Efficiency

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Output efficiency	MV12	87.0	-	-	%	V_{in} = 230 V AC, P_{out} = 90 W, T_A = 25°C, without a fan
		91.0	-	-		V_{in} = 230 V AC, P_{out} = 180 W, T_A = 25°C, without a fan
		94.0	-	-		V_{in} = 230 V AC, P_{out} = 450 W, T_A = 25°C, without a fan
		91.0	-	-		V_{in} = 230 V AC, P_{out} = 900 W, T_A = 25°C, without a fan

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
		87.0	-	-		V_{in} = 115 V AC/240 V DC, P_{out} = 200 W, T_A = 25°C, without a fan
		91.0	-	-		V_{in} = 115 V AC/240 V DC, P_{out} = 500 W, T_A = 25°C, without a fan
		89.0	-	-		V_{in} = 115 V AC/240 V DC, P_{out} = 900 W, T_A = 25°C, without a fan
	MV6	70.0	-	-		V_{in} = 230 V AC/240 V DC, I_{out} = 8 A, T_A = 25°C, without a fan

2.5 Protection Features

AC Input Protection

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
AC input overvoltage protection threshold	280	-	-	V	Self-recovery
AC input overvoltage recovery threshold	275	-	-	V	Hysteresis ≥ 5 V
AC input undervoltage protection threshold	-	-	85	V	Self-recovery
AC input undervoltage recovery threshold	-	-	90	V	Hysteresis ≥ 5 V (During recovery, the PSU cannot start in the hysteresis range)
AC input overcurrent or short circuit protection	-	-	-	-	Use a fast-blow fuse
PFC overvoltage protection	-			-	PFC overvoltage does not damage the bus capacitor (excluding damage caused by input overvoltage)

NOTE

1. If input overvoltage or undervoltage protection is triggered, MV12, SV12 and MV6 are shut down. The input voltage threshold that causes MV12 and SV12 to shut down are the same as the input voltage threshold that causes MV6 to shut down.
2. If input overvoltage or undervoltage is rectified, MV12, SV12 and MV6 recover. The input voltage threshold that causes MV12 and SV12 to recover are the same as the input voltage threshold that causes MV6 to recover.

HVDC Input Protection

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
HVDC input overvoltage protection threshold	310	-	-	V	Self-recovery
HVDC input overvoltage recovery threshold	305	-	-	V	Hysteresis ≥ 5 V
HVDC input undervoltage protection threshold	-	-	175	V	Self-recovery
HVDC input undervoltage recovery threshold	-	-	180	V	Hysteresis ≥ 5 V (During recovery, the PSU cannot start in the hysteresis range)
PFC overvoltage protection	-			-	PFC overvoltage does not damage the bus capacitor (excluding damage caused by input overvoltage)

NOTE

- If input overvoltage or undervoltage protection is triggered, MV12, SV12 and MV6 are shut down. The input voltage threshold that causes MV12 and SV12 to shut down are the same as the input voltage threshold that causes MV6 to shut down.
- If input overvoltage or undervoltage is rectified, MV12, SV12 and MV6 recover. The input voltage threshold that causes MV12 and SV12 to recover are the same as the input voltage threshold that causes MV6 to recover.

Output Protection

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Output overvoltage protection threshold	MV12	13	-	15	V	Latch off.

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
	MV6	13	-	15	V	Latch off. In the MV6 mode, if the PSU loop is detected to be open, protection is triggered directly without having to reach the MV6 overvoltage protection threshold.
	SV12	13	-	15	V	Latch off.
Output overcurrent protection threshold	MV12	110	-	130	%	100 ms minimum, latch off.
		130	-	150		4 ms minimum, latch off.
	MV6	11	13	15	A	• 100 ms minimum, the PSU outputs in MV12 mode. • The PSU can enter MV6 mode only after the PSON12V# signal changes from high level to low level, and then from low level back to high level.
	SV12	50	-	-	A	100 ms minimum, The PSU enters the MV12 mode after it experienced overcurrent in SV12 mode. The green indicator blinks at 1 Hz.
Output short circuit protection threshold	MV12	150	-	-	%	500 µs maximum, latch off.
	MV6	15	-	-	A	500 µs maximum, latch off.
	SV12	-	-	-	A	Latch off.

Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
Overtemperature protection	-	55	-	-	°C	• In the normal input range, the PSU can be protected against overtemperature and shut down only when the ambient temperature is higher than 55°C. Overtemperature protection can be automatically restored. The hysteresis for restoration must be greater than 5°C. • The environment protection threshold of the PSU must be set to 70°C or higher. • Overtemperature protection needs to be triggered for high internal component temperature caused by fan heat dissipation failure. • If the PSU experiences overtemperature in MV12 or SV12 mode, it will output based on MV6 mode. When the temperature restores to normal and the PSON12V# signal is at low level, the PSU can enter MV12 or SV12 mode. • If the PSU experiences overtemperature in MV6 mode, it will shut down output. When the temperature restores to normal, the PSU restores to MV6

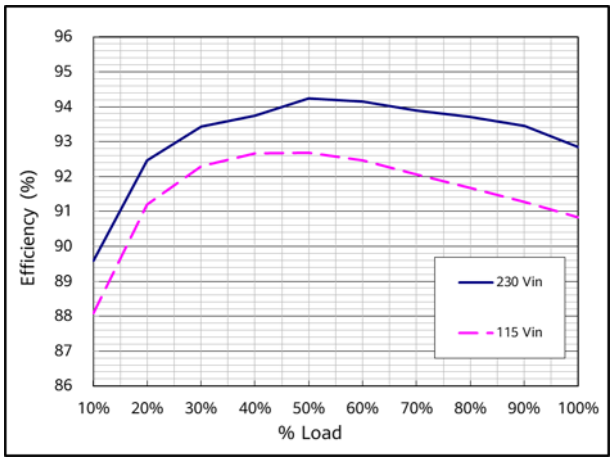
Parameter	Output	Min.	Typ.	Max.	Unit	Notes & Conditions
						mode first, and then restores to MV12 mode if the PSON12V# signal is at low level. The hysteresis for restoration must be greater than 5°C.

NOTE

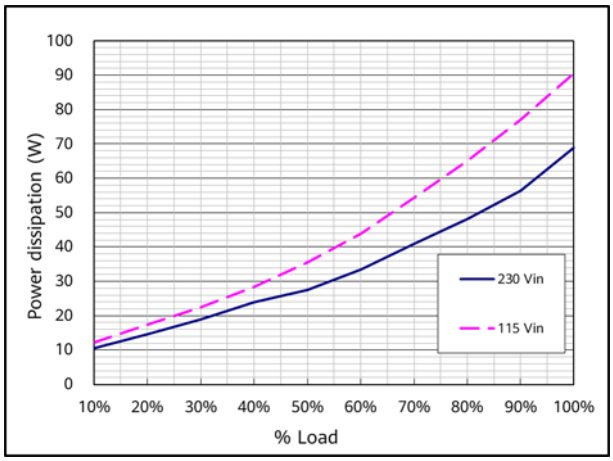
1. Unlatch mode of output overvoltage protection (the PSU unlatches if any of the following requirements is met): Input is recovered after AC power has failed for 15s; the INSTALLED# signal changes from low level to high level; the PSON12V# changes from high level to low level; the IP PRESENT# signal changes from low level to high level twice within 30s. When PSUs are working in parallel, if one of the PSUs triggers overvoltage protection and AC input is recovered after an AC power failure, the PSU can unlatch within 2s.
2. Unlatch mode of the MV12 output overcurrent/short circuit protection (the PSU unlatches if any of the following requirements is met): Input is recovered after AC power has failed for 15s; the INSTALLED# signal changes from low level to high level; the PSON12V# changes from high level to low level; the IP PRESENT# signal changes from low level to high level twice within 30s. When PSUs are working in parallel, if one of the PSUs triggers overcurrent protection and AC input is recovered after an AC power failure, the PSU can unlatch within 2s.
3. Unlatch mode of the SV12 output overcurrent/short circuit protection (the PSU unlatches if any of the following requirements is met): Input is recovered after AC power has failed for 15s; the INSTALLED# signal changes from low level to high level; when overcurrent occurs in SV12 mode but the PSU is not shut down, the IP PRESENT# signal changes from low level to high level once; when overcurrent occurs in SV12 mode and the PSU is shut down, the IP PRESENT# signal changes from low level to high level twice within 30s.
4. Unlatch mode of the MV6 output overcurrent/short circuit protection (the PSU unlatches if any of the following requirements is met): Input is recovered after AC power has failed for 15s; the INSTALLED# signal changes from low level to high level; the PSON12V# changes from high level to low level.
5. When the system needs to be unlatched, change the PSON12V# signal to high level for more than 500 ms and then change the PSON12V# signal to low level to ensure that the PSU can be unlatched reliably (mains overvoltage/overcurrent).
6. When the system needs to be unlatched, change the IP PRESENT# signal to low level for more than 500 ms and then change the IP PRESENT# signal to high level to ensure that the PSU can be unlatched reliably (overvoltage/overcurrent in SV12 mode).
7. When PSUs are working in parallel, if one of the PSUs triggers overvoltage or overcurrent protection and AC input is recovered after an AC power failure, the PSU can unlatch within 2s.
8. If the PSU enters protection state, MCU and I2C can work properly.
9. When the PSU triggers overload protection, there are no requirements on the output regulated voltage precision.
10. If the PSU changes from MV12 mode to MV6 mode, before the output voltage drops to 9 V, loads in MV12 mode are all disconnected and the PSU carries only the loads in MV6 mode.

3 Characteristic Curves

Conditions: T_A = 25°C unless otherwise specified



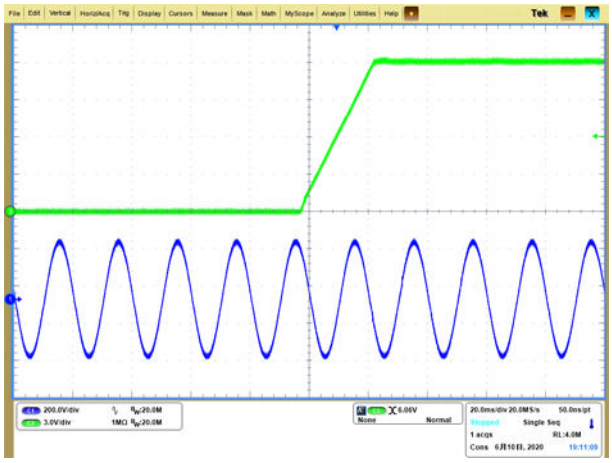
Efficiency curve, MV12



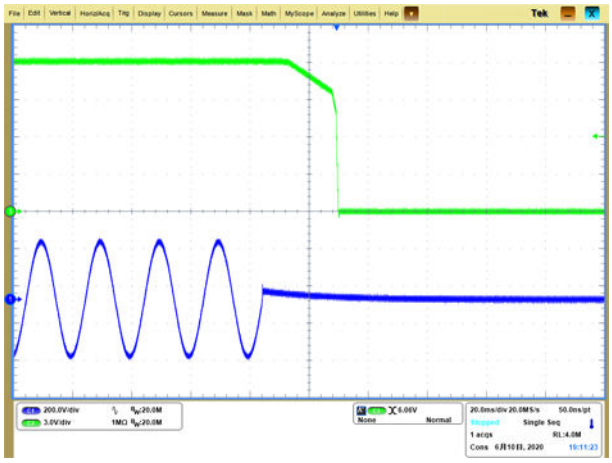
Power dissipation curve, MV12

4 Typical Waveforms

4.1 Turn-on/Turn-off

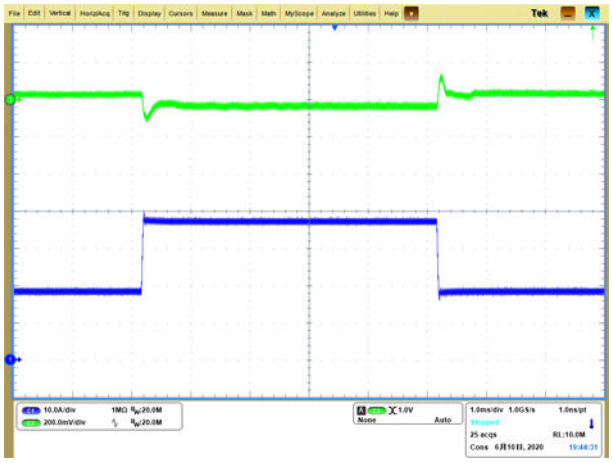


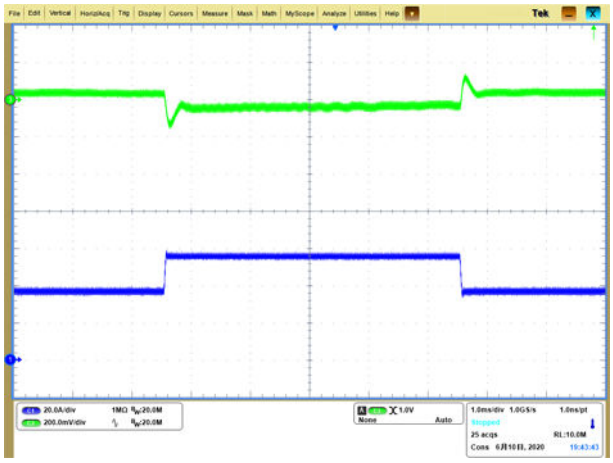
Turn-on for AC input (T_A = 25°C, V_{in} = 220 V AC, MV12, 100% load)



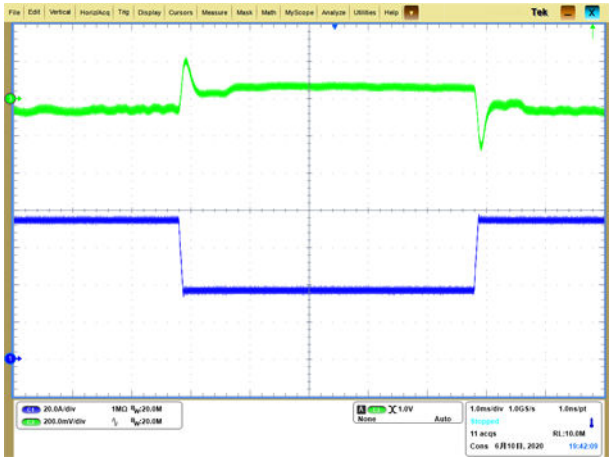
Turn-off for AC input (T_A = 25°C, V_{in} = 220 V AC, MV12, 100% load)

4.2 Output Voltage Dynamic Response

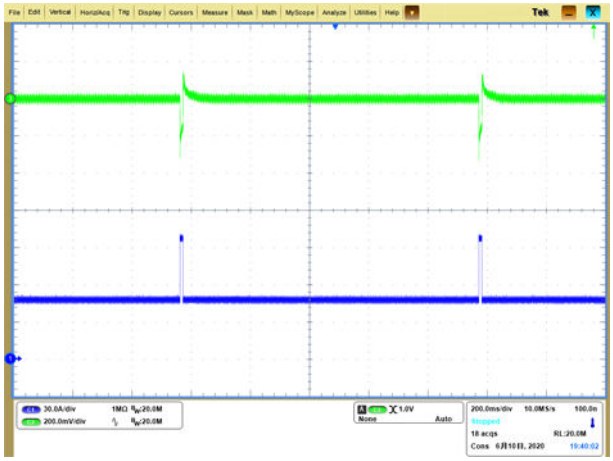




Output voltage dynamic response
(T_A = 25°C, V_{in} = 220 V AC, 25%–50%–25%, 0.5 A/µs, T = 10 ms, MV12)



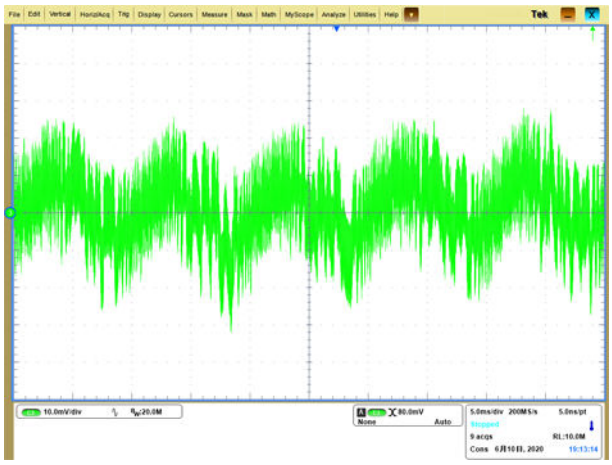
Output voltage dynamic response
(T_A = 25°C, V_{in} = 220 V AC, 50%–75%–50%, 0.5 A/µs, T = 10 ms, MV12)



Output voltage dynamic response
(T_A = 25°C, V_{in} = 220 V AC, 100%–50%–100%, 0.5 A/µs, T = 10 ms, MV12)

Output transient impact power overshoot
(T_A = 25°C, V_{in} = 220 V AC, 65%–130%–65%, 0.5 A/µs, pulse period 1s–10 ms–1s, MV12)

4.3 Output Voltage Ripple



T_A = 25°C, V_{in} = 220 V AC, MV12, 100% load

5 Energy Saving Feature

5.1 Active/Standby (Hot Standby) Power Supply

If PSUs work in parallel, PS_CONTROL (CEh) bit 7 is set to 1, the output voltage of the standby PSU is set to 12.05 V by 21h VOUT_COMMAND. The PSU with an output setting voltage of 12.3 V is the active PSU (only MV12 supports hot standby).

Table 5-1 Active/Standby power supply characteristics

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
12 V output voltage of the standby PSU	-	12.05	-	V	T_A = 25°C.
No-load power consumption of the standby PSU	-	-	5	W	1+1 power supply scenario: For the active/standby power supply with rated input of 115 V AC/230 V AC/240 V DC (AC+AC, AC+HVDC, HVDC+HVDC), the total input power is less than 75% of the rated output power of a single PSU and the input power consumption of each standby PSU is lower than 5 W.
	-	-	5	W	2+2 power supply scenario: For the active/standby power supply with AC+AC, AC+HVDC, or HVDC+HVDC, the total input power is less than 75% of the rated output power of two PSUs and the input power consumption of each standby PSU is lower than 5 W.

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Busbar voltage in fault mode	11.4	-	-	V	In 1+1 active/standby power supply scenarios (AC+AC, AC+HVDC, or HVDC +HVDC), if one of the PSUs powers off and experiences a fault (such as input power failure, input undervoltage, input overvoltage, fan fault, overtemperature, output overvoltage, or hot swap), the busbar 12 V voltage cannot be lower than 11.4 V, or the time when the voltage is lower than 11.4 V but not lower than 11 V cannot exceed 100 µs (excluding the scenario in which a short circuit occurs before ORing-FET). In a parallel scenario, the 12 V output is connected with a 540 µF capacitor.
	11.4	-	-	V	2+2 active/standby power supply scenario (AC+AC, AC+HVDC, or HVDC+HVDC): The 12 V mains voltage of the backplane bus cannot be lower than 11.4 V, or the time when the voltage is lower than 11.4 V but not lower than 11 V cannot exceed 100 µs, if any of the following faults occurs: 1. One power input fails (2+2 backup, one power input for two PSUs). 2. One of the PSUs experienced a fault (such as input undervoltage, input overvoltage, fan fault, overtemperature, output overvoltage, or hot swap). Note: 1. The 12 V output route has a 1500 µF capacitor. 2. In the 2+2 current sharing scenario, the total load should be less than or equal to 190% of the rated load of a single PSU. In the active/standby scenario, the total load should be less than or equal to 140% of the rated load of a single PSU.

5.2 Active/Standby N+R loading mode

In 1+1 mode, PSUs work in active/standby N+R mode. When the total load is less than or equal to 80% of the rated load of a single PSU, the standby PSU does not carry loads in stable state. When the total load is 80%–100% of the rated load of a single PSU, the load rate of the active PSU to the standby PSU does not exceed 6:1.

Table 5-2 N+R power supply specifications

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Output current for active/ standby switchover	-	-	20 ms @150%	%	• In 1+1 scenarios, the input voltage of the active PSU is 220 V/50 Hz, and that of the standby PSU is 230 V/50 Hz. The total load is between 50% and 100% of the load of a single PSU.
	-	-	100 ms @130%	%	
Output dynamics	11.4	-	13.3	V	• When the PSU load rate ranges from 80% to 100%, if an active/standby switchover occurs, the output voltage is allowed to drop within microseconds (less than 11.4 V/100 µs and greater than 11.0 V). The upper limit of the output voltage cannot exceed 13.3 V. • The input voltage of the active PSU is 220 V/50 Hz, and that of the standby PSU is 230 V/50 Hz.

NOTE

1. Provides a software interface for the system to query whether the N+R active/standby feature is supported. PS_CONTROL (CEh) bit 14 = 1 indicates that the N+R feature is supported. PS_CONTROL (CEh) bit 14 = 0 indicates that the N+R feature is not supported.
2. After the PSU enters the standby mode, it exits the standby mode only when one of the following occurs:
   - The system clears PS_CONTROL bit 7 of CEh.
   - The single-chip microcomputer of the PSU is powered off and then restarts.
   - A PSU communication fault occurs.
   - The output load exceeds the load capability of the standby PSU when a fault occurs (the load of the standby PSU exceeds 50% of the rated load).
   - The load of the active PSU exceeds 100%.
3. If the active PSU is faulty (except that the PSU is removed with power on and a short circuit occurs before the output ORing), the standby PSU needs to be woken up in a timely manner (false wakeup is allowed). The output voltage of the active PSU is allowed to drop within microseconds (less than 11.4 V/100 µs and greater than 11.0 V).
4. Restart requirements of the standby PSU (FF feature): The standby PSU restarts after the input power is off. If the DSP is not powered off, the status of the standby PSU is recorded. After the standby PSU starts, restart it at the standby PSU voltage (the input voltage of the active PSU is 220 V/50 Hz, and that of the standby PSU is 230 V/50 Hz).
5. After the program is updated on the standby PSU, the standby PSU is removed, the power communication fault is rectified, or the power module of the standby PSU is replaced, the active/standby information of the standby PSU is initialized (the active PSU is restored by default), and the system resets the active/standby information.
6. No single fault can cause the output voltage of the PSU to exceed the output overvoltage threshold.
7. Isolation function except for short circuits: The internal output overvoltage, overcurrent, short circuit, and short circuit modules can shut down the module output. If a PSU fails, it must be isolated reliably. When a single module fails, the system bus voltage overshoot (except internal short circuit and overvoltage) and the drop should meet the following requirements: The voltage should be greater than or equal to 11.4 V. When the load is greater than 80%, the voltage should be greater than or equal to 11.0 V, but the time when the voltage is lower than 11.4 V should be less than 100 µs.

5.3 Deep Sleep Function

The PSU enters deep sleep mode if bit B of PS_CONTROL (CEh) is set to 1. The deep sleep function is available in both MV12, SV12 and MV6 modes.

NOTE

When PSUs are connected in parallel, if one PSU enters deep sleep mode and the system communicates with it, the primary side information including input voltage, current, and power is reported as 0, and secondary side information is reported based on the actual situation (except that the output voltage and current are reported as 0).

Requirement

In deep sleep mode, the PSU input power is less than 1 W.

Acceptance criteria

1. The main power is shut down and 12 V has no output.

2. The PFC is shut down.
3. The fan obtains power from the 12 V bus.
4. The intelligent control function can be obtained through the 12 V bus.
5. The output of all PSU can be controlled online and restored to normal.

- In a parallel system, the PSU is not allowed to enter deep sleep mode unless all of the following occur:

1. The system sets the deep sleep control register to 1.
2. EFUSEV is less than or equal to 0.8 V.

- The PSU must be able to restore output of PSU when any of the following occurs:

1. The bus voltage is less than 5.7 V.
2. The system clears the deep sleep control register.
3. EFUSEV is greater than 1.0 V.

5.4 Cold Standby Energy Saving (Reserved)

In a redundancy system, cold standby mode is supported in PSU 1+1 scenarios when the output mode is MV12.

- The PSU can enter cold standby mode if all of the following conditions are met:

1. The system sends a D0h 0X01 command to set one of the PSUs as the active PSU. (Smart ON changes to high level)
2. The system sends D0h 0X02/0x03/0x04 to the other PSU and detects that Smart ON is high.
3. The load is less than 70% rated load of a single PSU.

- The cold standby PSU exits cold standby mode if any of the following conditions is met:

1. The system sends the D0h 0X00 command.
2. The single-chip microcomputer of the PSU restarts.
3. The I2C communication of the PSU is abnormal.
4. The 12 V output of the active PSU is faulty, such as input power failure, input overvoltage/undervoltage, output overvoltage/overcurrent/undervoltage (< 11.8 V), overtemperature, and fan fault, which causes Smart ON to change to low level.
5. The PSON12V# signal changes from low level to high level, and the INSTALLED# signal changes from low level to high level.
6. The load power is greater than the maximum power supported by cold backup.

- The active PSU exits cold standby mode if any of the following conditions is met:

1. The system sends the D0h 0X00 command.
2. The single-chip microcomputer of the PSU restarts.
3. The I2C communication of the PSU is abnormal.
4. The 12 V output of the active PSU is faulty, such as input power failure, input overvoltage/undervoltage, output overvoltage/overcurrent/undervoltage (< 11.8 V), overtemperature, and fan fault.

5. The PSON12V# signal changes from low level to high level, and the INSTALLED# signal changes from low level to high level.

Table 5-3 Standby PSU power consumption

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Standby PSU power consumption	-	-	5	W	Input voltage: 115 V AC/230 V AC/240 V DC In a 1+1 scenario (AC+AC, AC+HVDC, or HVDC+HVDC), the input power consumption of each standby is less than 5 W.

6 Hot Swap Requirements

During PSU hot swap, the PSU output voltage cannot exceed the PSU specifications.

The PSU can be hot swapped by the following methods:

1. PSU hot swap without AC power applied

   NOTE

   - The PSU does not work before the insertion or extraction.
   - Requirements should be met in both AC input and 240 V DC input scenarios.

   a. Extraction: Disconnect the AC power from the PSU, and then remove the PSU from the system.

   b. Insertion: The PSU is inserted into the system without power applied. Then, power is applied after the insertion.

2. PSU hot swap through the management system

   a. Extraction: The management system removes the PSU by turning off the PSON12V# signal.

   b. Insertion: After a PSU is inserted into the system, the system processor queries the PSU based on the system status (on or off) and then enables the mains mode of the PSU using the PSON12V# signal.

3. PSU hot swap with AC power applied

   NOTE

   Requirements should be met in both AC input and 240 V DC input scenarios.

   a. Extraction: The PSU is removed when it is working properly.

   b. Insertion: The PSU starts immediately after it is inserted into the system.

7 Internal Cooling Fan

The PSU supports forcible air cooling by drawing air. It draws air in from the rear panel and blows air out from the front panel.

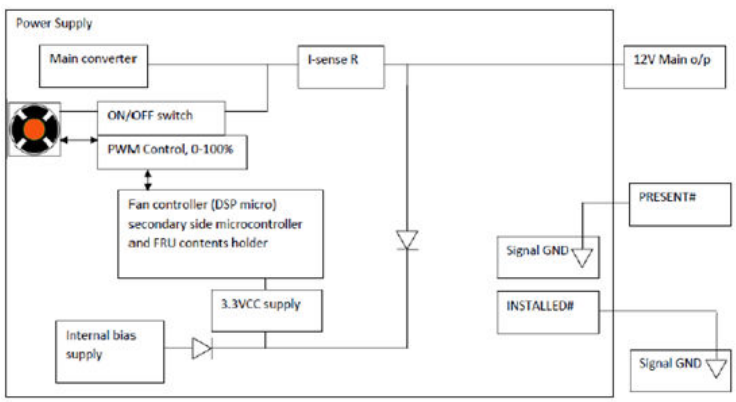
Heat Dissipation Requirements

1. In MV6 mode, the PSU will not trigger overtemperature protection when the fan works at the lowest speed.
2. In MV12 mode, the PSU will not trigger overtemperature protection when the fan works at the preset speed.
3. The fan cannot stop rotating in the case of reverse power supply.
4. Before overtemperature protection, the fan must operate at full speed.
5. When the temperature at the air intake vent of the PSU reaches 45°C, the fan speed can be adjusted.

Fan Power Supply Mode

1. The fan obtains power from the output bus. A fan fault cannot cause a system alarm or reset. The bus voltage must be greater than or equal to 11.0 V and the time when the bus voltage is lower than 11.4 must not exceed 100 µs.
2. The fan should be isolated if a fault occurs.
3. The system can deliver a command to turn off the fan.

Figure 7-1 Fan power supply circuit



Noise Requirements

Table 7-1 PSU noise

Parameter	Max.	Notes & Conditions	Remarks
PSU noise	50 dB	Air inlet temperature 25°C, noise sensor 1 m away from the PSU, 40% load	The noise sensor should face the air exhaust vent of the fan.

Fan Protection

1. If PSUs are connected in parallel and one of the fans or the power supply circuit is short-circuited or open-circuited, the 12 V and 6 V routes of the system backplane should not exceed the normal dynamic change voltage restriction specifications. The system operation should not be affected.
2. The fan fault detection circuit can report a fault only when it detects a fan or fan circuit fault and the fault lasts for over 20s. (Long-time fan operation ages the internal bearing, which prolongs fan startup time. The fan is considered to be faulty only when it does not reach the specified rotational speed after more than 20s.)
3. A fan fault can be rectified.

8 Parallel Operation

Current Share Design Requirements

1. Supports 1+1 or 2+2 mode. Current sharing only in MV12 mode.
2. The total load at startup in parallel operation scenarios should be less than the rated load of a single PSU.
3. When PSUs work in 1+1 or 2+2 mode, if one of the PSUs works in MV6 mode and other PSUs work in MV12 mode, the PSUs should work properly without affecting each other.
4. In scenarios where different PSUs are not installed together, the I-MON signals of the two PSUs should not affect the normal operation of the PSUs when they are directly connected.
5. Current sharing imbalance only in the normal temperature condition.

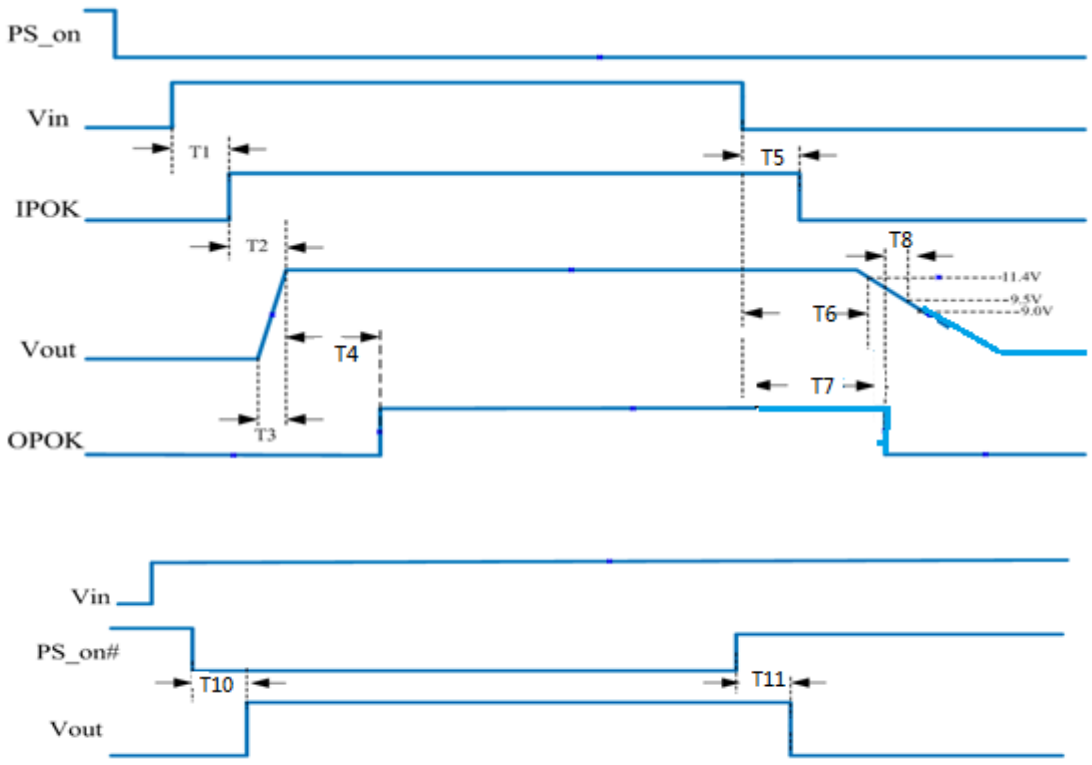
PSU Mixture Requirements

1. The PSU should meet system application requirements when it is installed together with the PAC900S12-B1 server power module.
   a. In MV12 mode, the current sharing imbalance is 10% within the range of 50%–100% rated output load.
   b. In MV12 mode, the current sharing imbalance is 15% within the rated output load range of 200 W to 50%.
   c. Current sharing balance is not required when the power is less than 200 W.
2. The PSU should not be damaged when it is used with the PAC2000S12-BG, PAC1500S12-BE, and PAC550S12-BE AC power modules.
3. The active/standby mode does not support mixed insertion.
4. The cold standby mode does not support mixed insertion.

9 Control Functions

9.1 Timing Requirements

Figure 9-1 PSU timing diagram



Mark	Description	Min.	Max.	Unit
T1	Time from AC/DC input to when IPOK becomes high level	-	2000	ms
T2	Time from when IPOK becomes high level to when MV12 output to 11.4 V	-	500	ms
T3	Time for MV6 output to increase from 10% to 90%	5	25	ms

Mark	Description	Min.	Max.	Unit
	Time for MV12 output to increase from 10% to 90%	5	25	ms
T4	Delay time for the OPOK to take effect (when MV12/MV6 increases to 90% to when OPOK is at high level)	50	100	ms
T5	IPOK failure delay time (from input outage to low IPOK signal, circuit breaker disconnection not considered, full load test conditions)	-	4	ms
T6	Output hold-up time 1 (from input power failure during normal running to 11 V output, 100% load, DIP performance)	10	-	ms
T7	OPOK hold-up time (normal working input power failure to low OPOK signal, 100% load).	10	-	ms
	Time from when the AC power fails to when the OPOK signal becomes low level: 50% load	20	-	ms
	Time from when the AC power fails to when the OPOK signal becomes low level: 20% load	30	-	ms
	Time from when the AC power fails to when the OPOK signal becomes low level: 10% load	40	-	ms
T8	Duration from the time when the OPOK signal falls to 1.43 V to the time when the 12 V bus voltage drops to 9.5 V	200	-	µs
T9	Output hold-up time 2 (from low IPOK signal to when the output drops to 5.7 V after input power failure during normal running. When the output voltage is lower than 9.2 V, the output power is 15 W. T6 is considered and power failure logs are recorded.)	300	-	ms
T10	PSON delay when the PSU switches from MV6 to MV12 mode (from when PSON becomes low level to when the output voltage is 11.4 V)	80	200	ms
	Time from MV6 output to 11 V when MV6 OCP and MV12 OTP recover	2.1	3.3	s
T12	PSON delay when the PSU switches from MV12 to MV6 mode (from high PSON signal to MV6 output upper limit, 24 W)	80	200	ms

NOTE

1. In case of input power failure, the PSU needs 10–120 ms to set IIC alarm position to 1 at more than half load, and the system needs 20–120 ms to set IIC alarm position to 1 at below half load (including half load).
2. The storage NVDIMM power backup requirement is supported.

   For T8 Only: This is required in the case of input power failure, input overvoltage/undervoltage, fan fault, and overtemperature, and is not required in the case of OPOK alarms caused by output overcurrent/short-circuit and output overvoltage; if input power failure, undervoltage, or overvoltage occurs, the OPOK voltage should not rebound after dropping.

   The PSU can report the OPOK fault in advance if the fault can be predicted by the PSU (such as input power failure, input overvoltage/undervoltage, fan fault, overtemperature, or output undervoltage). In this case, the requirement that the output voltage must be less than 11.4 V does not have to be met.
3. The test of T1 and T2 requires that the auxiliary power supply be completely powered off.
4. Test T3 when the load is higher than the minimum value.

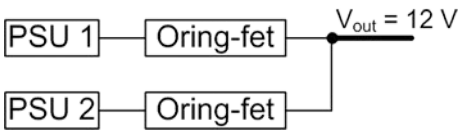
9.2 ORing-FET

An ORing-FET failure isolation circuit needs to be added to the PSU MV12 output. In the parallel scenario (1+1/2+2 backup), if one PSU experiences an internal fault, it should exit automatically to prevent the bus voltage output from being abnormal.

NOTE

- Capacitance at the MV12 input side: The equivalent capacitance should be greater than the PSU's minimum capacitive load 540 μF multiplied by N (N is the number of PSUs configured in the system) and less than the PSU's maximum capacitive load 22000 μF.
- The MV12 load should be greater than the minimum PSU load 3 A and less than the rated load of the PSU.

Figure 9-2 ORing-FET circuit



9.3 PSON12V#

The PSON12V# signal is an on/off signal that controls the PSU MV12 output remotely. If the PSON12V# signal is at low level, the PSU enters MV12 output mode. If the PSON12V# is at high level or not connected, the PSU enters MV6 output mode.

NOTE

- When PSON# is at high level or left open, the PSU output mode is switched from MV12 to MV6.
- If PSON# is at high level for 25 ms or longer, PSON# is valid.

Figure 9-3 Interconnect diagram of the PSON12V# signal

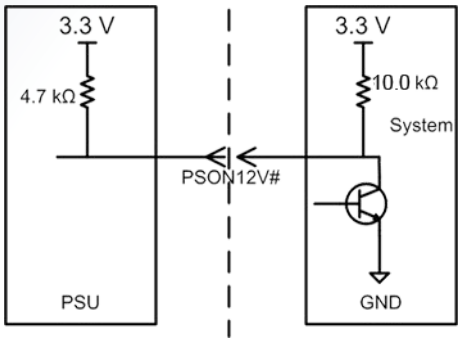


Table 9-1 PSON12V# signal characteristics

Signal Characteristics	
Signal type:PSU on/off signal	PSU side: This signal is pulled up to the 3.3 V auxiliary power source inside the PSU through a pull-up resistor (reference value: 4.7 kilohms). System side: This signal is output by CPLD over the drive circuit and pulled up to 3.3 V by a 10-kilohm resistor.
PSON12V# = Low	MV12 output mode.
PSON12V# = High/Not connected	MV6 output mode.

Table 9-2 PSON12V# output

PSON12V# Output	Min.	Max.
Low level voltage (main output enabled)	0 V	0.8 V
High level voltage (main output disabled)	2.000 V	3.465 V
Source current, Vpson = Low	-	4 mA
Signal rise and fall time	-	200 μs

9.4 PRESENT#

The PRESENT# signal is used by the system to detect whether the PSU is present. The signal pin is required to be shorter than other pins on the PSU. The signal is grounded inside the PSU.

PSU side: The signal is directly grounded inside the PSU.

System side: This signal is pulled up to 3.3 V by a 4.7-kilohm resistor and output to the system CPLD over a series resistor.

9.5 INSTALLED#

The INSTALLED# signal is used by the PSU to determine whether it has been inserted into the system. The signal pin is required to be shorter than other pins on the PSU. High level indicates that the PSU has not been inserted into the system and low level indicates that the PSU has been inserted into the system. When the INSTALLED# signal pin is left open, the PSU has no output. When inserted into the system, the PSU starts main output mode.

Table 9-3 INSTALLED# signal characteristics

Signal Characteristics	
Signal type: The PSU determines whether it has been inserted into the system.	PSU side: This signal is pulled up to the 3.3 V auxiliary power source inside the PSU through a pull-up resistor (reference value: 4.7 kilohms). System side: This signal is grounded directly.
INSTALLED# = Low	The PSU is inserted into the system.
INSTALLED# = High	The PSU is not inserted into the system.

Table 9-4 INSTALLED# output

INSTALLED# Output	**Min.**	**Max.**
Low level voltage (main output enabled)	0 V	0.8 V
High level voltage (main output disabled)	2.000 V	3.465 V
Input sink current, INSTALLED# = Low	-	4 mA
Signal rise and fall time	-	200 µs

9.6 OPOK#

The OPOK# signal indicates whether the main output is normal.

Figure 9-4 Interconnect diagram of the OPOK# signal

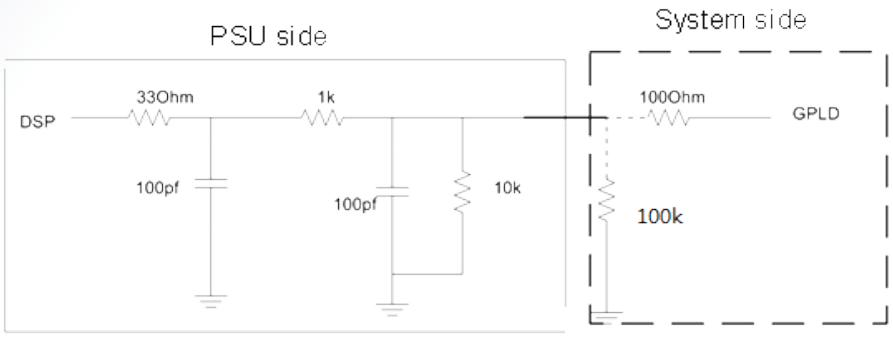


Table 9-5 OPOK# signal characteristics

Signal Characteristics	
Signal type	PSU side: The DSP is output to the edge connector after RC filtering. System side: Pulled down to GND by a 100-kilohm resistor and connected to the system CPLD over a 100-ohm series resistor.
OPOK# = High	The main output is normal.
OPOK# = Low	The main output is abnormal.

Table 9-6 OPOK# output

OPOK# Output	**Min.**	**Max.**
Low level voltage	0 V	0.6 V
High level voltage	2.200 V	3.465 V
Sink current, OPOK# = Low	-	4 mA
Signal rise and fall time	-	200 µs

NOTE

1. If the INSTALLED# signal is at high level, then the OPOK signal is at low level.
2. In MV12 mode:
   1. V_{out} > 11.5 V, OPOK is at high level.
   2. V_{out} < 11.4 V, OPOK is at low level.
   3. The time from when OPOK drops to 1.43 V to when the 12 V bus voltage drops to 9.5 V is greater than 200 µs (this is required in case of input power failure, input overvoltage/undervoltage, fan fault, overtemperature, and output undervoltage, and is not required in scenarios such as output overcurrent or short circuit and output overvoltage).
3. In MV6 mode:
   1. V_{out} > 5.9 V, OPOK is at high level.
   2. V_{out} < 5.8 V, OPOK is at low level.
4. In case of input power failure, input overvoltage, input undervoltage, fan fault, overtemperature, and output undervoltage, the PSU can report the OPOK fault in advance.
5. After the input power fails, the OPOK signal changes to low level. The OPOK signal should not changes to high level until the input power recovers.

9.7 IPOK#

The IPOK# signal is used to detect whether the PSU input is normal.

Figure 9-5 Interconnect diagram of the IPOK# signal

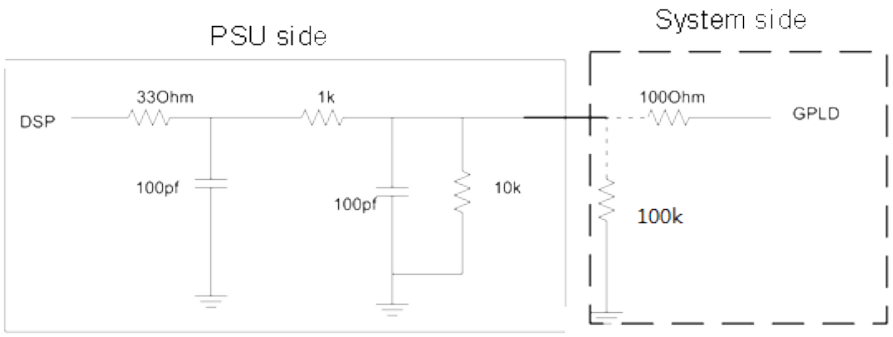


Table 9-7 IPOK# signal characteristics

Signal Characteristics	
Signal type	PSU side: The power is output after RC filtering. System side: Pulled down to GND by a 100-kilohm resistor and connected to the system CPLD over a 100-ohm series resistor.
IPOK# = High	The input is normal. (90 V AC < V_{in} < 264 V AC; 180 V DC < V_{in} < 300 V DC)
IPOK# = Low	The input is abnormal (after AC or DC input undervoltage/overvoltage protection).

Table 9-8 IPOK# output

IPOK# Output	Min.	Max.
Low level voltage	0 V	0.6 V
High level voltage	2.200 V	3.465 V
Sink current, IPOK# = Low	-	4 mA
Source current, IPOK# = High	-	4 mA
Signal rise and fall time	-	200 µs

9.8 IPOK LINK#

The IPOK LINK# signal is sent by the system to the PSU. It indicates that at least one PSU is present in the system and its input is normal. This signal is for function extension.

Table 9-9 IPOK LINK# signal characteristics

Signal Characteristics	
Signal type	PSU side: This signal is pulled up tothe 3.3 V auxiliary power source inside the PSUthrough a pull-up resistor (reference value: 2.49 kilohms). System side: This signal is output by CPLD over the drive circuit and pulled up to 3.3 V by a 4.7-kilohm resistor.
IPOK LINK# = High	The standby power supply input is normal.
IPOK LINK# = Low	The standby power supply input is abnormal.

Table 9-10 IPOK LINK# output

IPOK LINK# Output	Min.	Max.
Low level voltage	0 V	0.6 V
High level voltage	2.200 V	3.465 V
Sink current, IPOK LINK# = Low	-	4 mA
Source current, IPOK LINK# = High	-	4 mA
Signal rise and fall time	-	200 µs

9.9 IP PRESENT#

IP PRESENT# is an active-low signal that controls the SV12 switch of the PSU. After IP PRESENT is valid, the PSU enters the SV12 output state. The designed overcurrent protection threshold is greater than or equal to 50 A in this case. When the PSON12V# signal is at high level, the PSU maintains the MV12 output mode.

Table 9-11 IP PRESENT# signal characteristics

Signal Characteristics	
Signal type	PSU side: This signal is pulled up to the 3.3 V auxiliary power source inside the PSU through a pull-up resistor (reference value: 4.75 kilohms). System side: This signal is output by CPLD over the drive circuit and pulled up to 3.3 V by a 4.7-kilohm resistor.
IP PRESENT# = High	The PSU does not act.
IP PRESENT# = Low	The PSU enters the SV12 output mode.

Table 9-12 IP PRESENT# output

IP PRESENT Output	**Min.**	**Max.**
Low level voltage	0 V	0.6 V
High level voltage	2.000 V	3.465 V
Sink current, IP PRESENT# = Low	-	4 mA
Source current, IP PRESENT# = High	-	4 mA
Signal rise and fall time	-	200 µs

9.10 CYC_PWR#

The CYC_PWR# signal is sent to PSUs by the system to shut down or restore the **MV12** output of the PSU.

- The signal is valid if the CYC_PWR# signal is at low level for 100–150 ms. The PSU shuts down after the delay time (configurable) and then starts after the restart time (configurable).
- The CYC_PWR# signal is invalid if both the OPOK# and CYC_PWR# signals are low level.
- The signal is invalid if the CYC_PWR# signal is at low level for less than 100 ms.
- The CYC_PWR# signal is invalid when a PSU is during delay shutdown or restarting. The CYC_PWR# signal is valid after the OPOK signal becomes high level.

Table 9-13 CYC_PWR# signal characteristics

Signal Characteristics	
Signal type	PSU side: This signal is pulled up to the 3.3 V auxiliary power source inside the PSU through a pull-up resistor (reference value: 2.49 kilohms). System side: This signal is output by CPLD over the drive circuit and pulled up to 3.3 V by a 4.7-kilohm resistor.
CYC_PWR# = High	The PSU does not act.
CYC_PWR# = Low	The PSU enters power supply cycle power mode.

Table 9-14 CYC_PWR# output

CYC_PWR# Output	Min.	Max.
Low level voltage	0 V	0.8 V
High level voltage	2.000 V	3.465 V
Sink current, CYC_PWR# = Low	-	4 mA
Source current, CYC_PWR# = High	-	4 mA
Signal rise and fall time	-	200 µs

9.11 I_MON#

This signal is an MV12 output current sharing signal.

PSU Side	System Side
Internal current sharing bus	The backplane directly connects the I_MON# signals of all PSUs together.

9.12 PS_INTERRUPT#

The PS_INTERRUPT# signal indicates PSU I2C alarm interruption. High level indicates that the PSU is normal and low level indicates that the PSU has triggered an alarm.

Table 9-15 PS_INTERRUPT# signal characteristics

Signal Characteristics	
Signal type	PSU side: Output over the drive circuit, no pull-up on the PSU side. System side: Pulled up to 3.3 V level and then reversely sent to the system over the MOS transistor.
PS_INTERRUPT# = High	The PSU is normal.
PS_INTERRUPT# = Low	The PSU has triggered an alarm.

9.13 EFUSEV#

The system samples the input current of the main service load branch (12 V), converts the current to a linear voltage analog signal, and sends the signal to the EFUSEV pin of the PSU. If the value of EFUSEV is greater than 1.0 V, the main service of the system is working. In this case, the PSU cannot enable deep sleep and automatic PFC shutdown. If the value of EFUSEV is less than 0.8 V, the main service of the system is powered off or does not work. In this case, the PSU can enable deep sleep and automatic PFC shutdown.

Table 9-16 EFUSEV# signal characteristics

Signal Characteristics	
Signal type	PSU side: Sent to the PSU DSP by a 100-ohm series resistor. System side: • If this function is enabled, the system sends the voltage analog signal of the main service circuit to the PSU, or CPLD outputs this signal over the drive circuit and this signal is pulled up to 3.3 V level by a 4.7-kilohm resistor. • If this function is disabled, this signal is pulled up to 3.3 V level by a 4.7-kilohm resistor.
EFUSEV# = High	Disable deep sleep and automatic PFC shutdown
EFUSEV# = Low	Enable deep sleep and automatic PFC shutdown

Table 9-17 EFUSEV# output

EFUSEV# Output	Min.	Max.
Low level voltage	0 V	0.8 V
High level voltage	1.000 V	3.465 V

9.14 SMART_ON#

The SMART_ON# signal is used to wake up a cold-standby PSU (low level by default).

1. Active PSU setting: The system sends the D0h 0X01 command to the active PSU, the SMART_ON signal of the active PSU changes to high level, and then the PSU enters cold standby mode.
2. Standby PSU setting: The system sends the D0h 0X02/0X03/0X04 command to the standby PSU, and then the standby PSU disconnects the DC/DC circuit.
3. Standby PSU wake-up: If the active PSU is faulty and the SMART_ON signal changes to low level, the standby PSU starts working.

Table 9-18 SMART_ON# signal characteristics

Signal Characteristics	
Signal type: Cold-standby PSU wake-up signal	The SMART_ON# signals of all PSUs are connected together.
SMART_ON# = High	The PSU enters cold standby mode.
SMART_ON# = Low	The PSU exits from cold standby mode.

Table 9-19 SMART_ON# output

SMART_ON# Output	**Min.**	**Max.**
Low level voltage	0 V	0.8 V
High level voltage	2.0 V	3.6 V

10 Communication

10.1 Data Link Layer Protocol

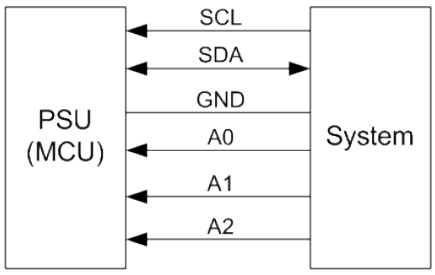
The link layer uses the PMBus V1.2 protocol and complies with *PMBus_Specification_Part_I_Rev_1-2_20100906* and *PMBus_Specification_Part_II_Rev_1-2_20100906*.

10.1.1 I2C Signal

The PSU includes a main control unit (MCU) used for monitoring and a DFlash used for storing fault records. The PSU can use the DFlash in the MCU to store fault records. The system sends commands to the MCU over the I2C bus to read fault records from the PSU.

Figure 10-1 shows the I2C interface communication diagram.

Figure 10-1 I2C interface



10.1.2 I2C Address

Addresses A2, A1, and A0 are allocated to a PSU. If this signal is connected to GND through a 300-ohm resistor, the address bit is 0. If this signal is left open, the address bit is 1. The I2C address of the PSU from high to low is A2, A1, and A0. See **Table 10-1** for details.

Table 10-1 I2C address

PSU A2/A1/A0	0/0/0	0/0/1	0/1/0	0/1/1	1/0/0	1/0/1	1/1/0	1/1/1
MCU	0xB0	0xB2	0xB4	0xB6	0xB8	0xBA	0xBC	0xBE

10.1.3 SCL and SDA

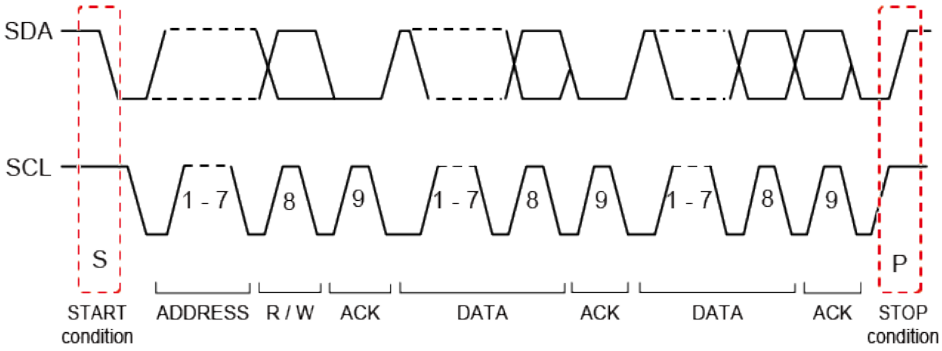
The I2C serial clock signal (SCL) and serial data signal (SDA) occupy two signal pins of the output connector.

PSU Side	System Side
• SCL and SDA are pulled up to 3.3 V level by a 20-kilohm resistor. • The supply voltage source for the secondary-side MCU is generated from the PSU auxiliary power supply and 12 V at the system side at the same time. • When power is supplied from the system side, there should be a fuse or an overcurrent or short circuit protection circuit. • Capacitors on the SCL and SDA circuit are no more than 66 pF.	SCL and SDA are pulled up to 3.3 V level by a 3-kilohm to 10-kilohm equivalent resistor.

10.1.4 Data Transmission Mode

The I2C transmission standard is used. The default clock frequency allowed by the I2C is 100 kbit/s. The timing definition of lower-layer signals, such as START, STOP, R/W, ADDRESS, ACK/NACK, bus arbitration, clock synchronization, and clock extension (except bus timeout) complies with PSMI.

Figure 10-2 I2C data transmission mode



10.1.5 I2C Bus Timeout

The I2C program of the PSU is reset to 0 if the PSU detects that the SCL or SDA data line is held low for more than 300 ms.

10.2 Network Layer Protocol

10.2.1 Slave Addressing Method

The PSU serves as the slave device, and the PSU address is identified by the hardware and assigned in static mode. The master device accesses slave devices independently based on the slave device addresses determined by the hardware.

10.2.2 Checksum

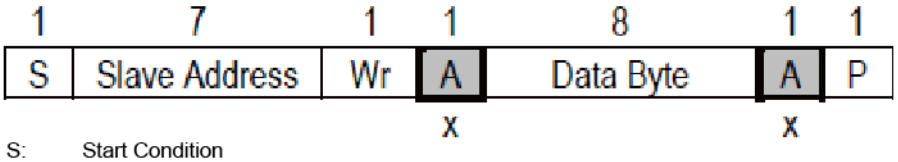
To ensure data integrity and accuracy during communication, the PSU uses the 8-bit CRC checksum mechanism.

The last byte sent for each communication is the CRC checksum for the communication data. For example, the last byte of the data returned by the PSU is the checksum.

The CRC checksum is generated using the multinomial: CRC8.

10.2.3 Data Transmission

PMBus communication supports 10 data formats in total. All data formats adopt PEC verification.

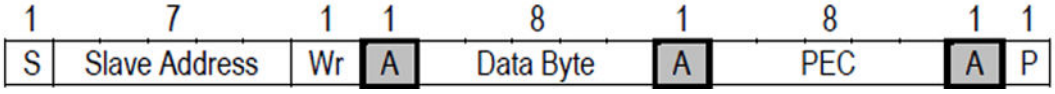


S: Start Condition
Sr: Repeated start condition
Rd: Read (bit value of 1)
Wr: Write (bit value of 0)
x: Shown under a field indicates that field is required to have the value of 'x'
A: Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P: Stop condition
PEC: Packet Error Code
...: Continuation of protocol

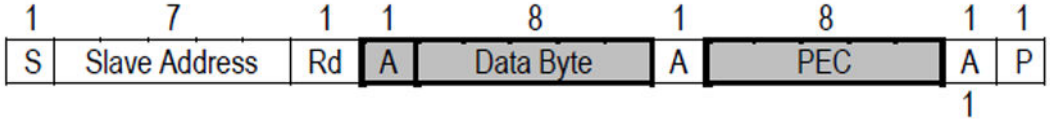
Master-to-Slave

Slave-to-Master

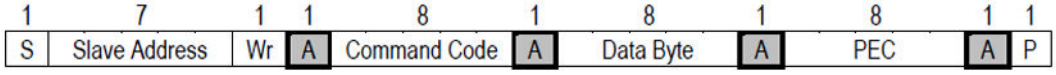
1. Send Byte command and response



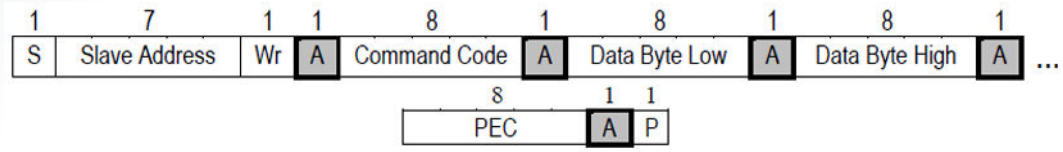
2. Receive Byte command and response



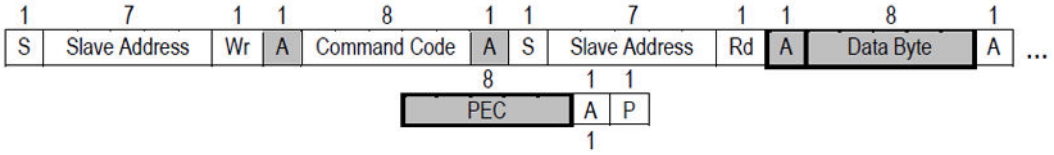
3. Write Byte command and response



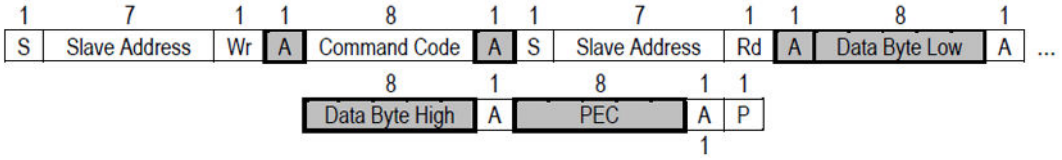
4. Write Word command and response



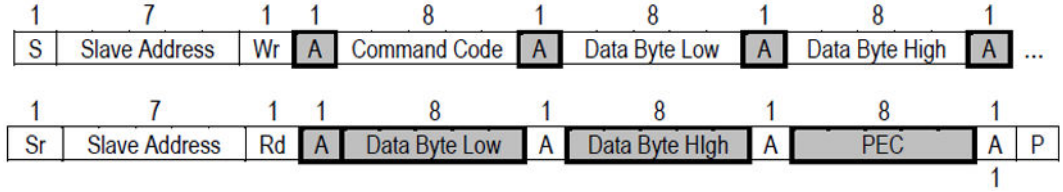
5. Read Byte command and response



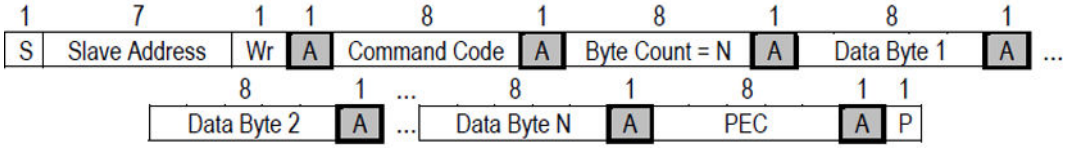
6. Read Word command and response



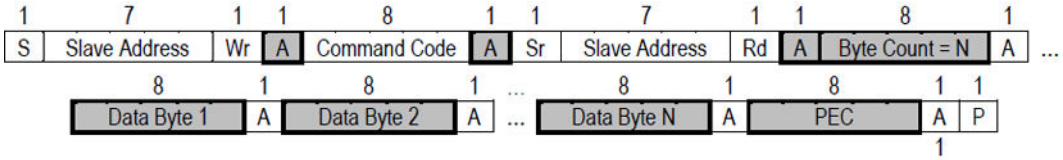
7. Process Call command and response



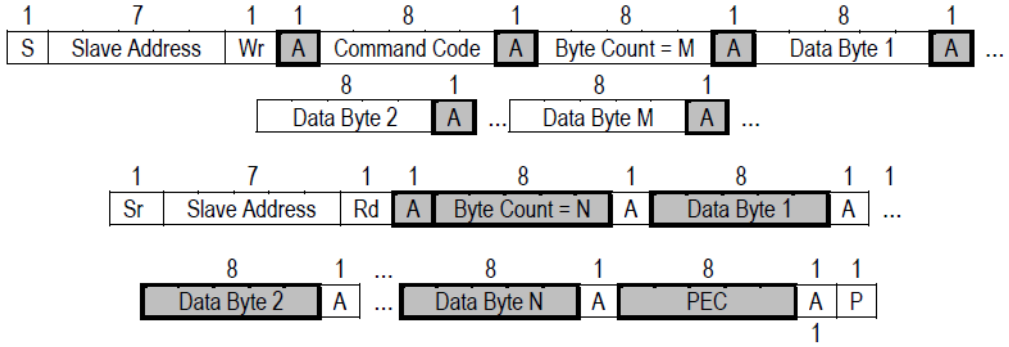
8. Block Write command and response



9. Block Read command and response



10. Block Read – Block Write Process Call command and response



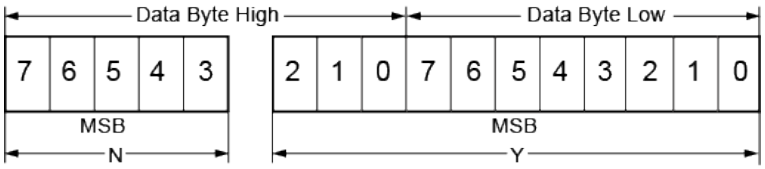
10.3 Application Layer Protocol

10.3.1 Data Format

Linear 11 Data Format

The linear data format is a two byte value with an 11-bit binary signed mantissa (two's complement) and a 5-bit binary signed exponent (two's complement), as shown in the following figure.

Figure 10-3 Linear 11 data format



The relationship between N, Y, and actual value X is given by the following equation:

$$X = Y \times 2^{N}$$

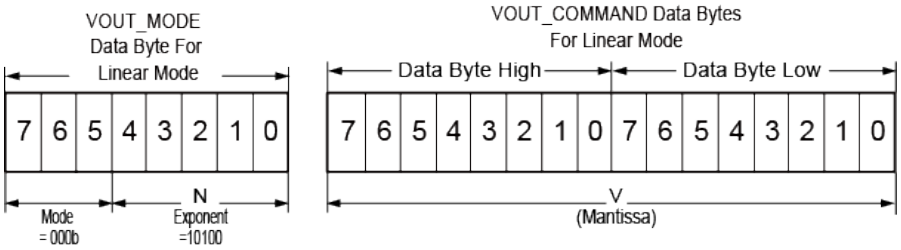
Where:

- Y is the 11-bit, binary signed mantissa (two's complement).
- N is the 5-bit, binary signed exponent (two's complement).

VOUT Data Format

Commands related to output voltage are VOUT_MODE and READ_VOUT. They are unsigned integers using the linear 16 format, as shown in the following figure.

Figure 10-4 VOUT data format



The output voltage is calculated as follows:

$$Voltage = V \times 2^{N}$$

Where:

- Voltage is the output voltage value.
- V is the 16-bit unsigned integer.
- N is the 5-bit signed integer (two's complement). N = –12.

10.3.2 Commands

Hex Code	Command Name	Description	Data Type	Data Format
0x01h	OPERATION	Remote startup and shutdown	Read/Write Byte	HEX
0x03h	CLEAR_FAULTS	Clearing faults	Write Byte	HEX
0x20h	VOUT_MODE	Output mode	Read Byte	HEX
0x21h	VOUT_CTRL	Output voltage configuration	Read/Write Word	Linear16
0x31h	RATED_POUT	Maximum output power	Read Word	Linear11
0x3Ah	FAN_CONFIG	Fan configuration	Read/Write Byte	HEX
0x3Bh	FAN_COMMAND	Fan speed setting	Read/Write Word	HEX
0x78h	STATUS_BYTE	Status single-byte	Read/Write Byte	HEX
0x79h	STATUS_WORD	Status dual-byte	Read/Write Word	HEX
0x7Ah	STATUS_VOUT	Output voltage status	Read/Write Byte	HEX
0x7Bh	STATUS_IOUT	Output current status	Read/Write Byte	HEX
0x7Ch	STATUS_INPUT	Input status	Read/Write Byte	HEX
0x7Dh	STATUS_TEMP	Temperature status	Read/Write Byte	HEX
0x7Eh	STATUS_CML	CMD status	Read/Write Byte	HEX
0x80h	STATUS_MFR_SPECIFIC	MFR status	Read/Write Byte	HEX
0x81h	STATUS_FANS	Fan status	Read/Write Byte	HEX
0x88h	READ_VIN	Input voltage	Read Word	Linear11
0x89h	READ_IIN	Input current	Read Word	Linear11
0x8Bh	READ_VOUT	Output voltage	Read Word	Linear16
0x8Ch	READ_IOUT	Output current	Read Word	Linear11
0x8Dh	READ_TEMPERATURE_1	Ambient temperature	Read Word	Linear11

Hex Code	Command Name	Description	Data Type	Data Format
0x8Eh	READ_TEMPERATURE_2	Primary side temperature	Read Word	Linear11
0x8Fh	READ_TEMPERATURE_3	Secondary side temperature	Read Word	Linear11
0x90h	READ_FAN_SPEED	Fan speed	Read Word	DEC
0x95h	READ_FREQUENCY	PSU frequency	Read Word	Linear11
0x96h	READ_POUT	Output power	Read Word	Linear11
0x97h	READ_PIN	Input power	Read Word	Linear11
0x98h	PMBUS_REVISION	PMBus version	Read Byte	DEC
0x99h	MFR_ID	Vendor name	Read Block	ASCII
0x9Ah	MFR_MODEL	PSU name	Read/Write Block	ASCII
0x9Bh	HARD_VERSION	Hardware version	Read Block	ASCII
0x9Dh	MFR_DATE	Production date	Read/Write Block	ASCII
0x9Eh	MFR_SERIAL	Product SN	Read/Write Block	ASCII
0xBDh	E_LABLE_LENGTH	Length and frame length of the e-label	Read/Write Block	HEX
0xBEh	E_LABLE_INDEX	E-label number	Read/Write Word	DEC
0xBFh	E_LABLE_CONTENT	E-label content	Read/Write Block	ASCII
0xC0h	POWER_CYCLE_TIME	Shutdown delay time	Read/Write Word	DEC
0xC6h	WARNING_COUNT1	Alarm counter 1	Read/Write Word	DEC
0xC7h	WARNING_COUNT2	Alarm counter 2	Read/Write Word	DEC
0xC8h	WARNING_COUNT3	Alarm counter 3	Read/Write Word	DEC
0xCCh	MAX_VIN	Maximum input voltage	Read/Write Word	Linear11
0xCDh	MAX_IIN	Maximum input current	Read/Write Word	Linear11
0xCEh	PS_CONTROL	PSU control register	Read/Write Word	HEX
0xCFh	READ_POWER_TYPE	PSU type	Read Word	HEX

Hex Code	Command Name	Description	Data Type	Data Format
0xD0h	SMART_ON_CONFIG	Cold standby configuration command	Read/Write Byte	HEX
0xD4h	SET_PSALERT	Forcible alarm command	Read/Write Byte	HEX
0xD6h	MAX_PIN	Maximum input power	Read/Write Word	Linear11
0xD7h	MAX_POUT	Maximum output power	Read/Write Word	Linear11
0xD8h	MAX_TEMP_MONITOR	Maximum temperature of the PSU air intake vent	Read/Write Word	Linear11
0xDBh	MAX_12V_IOUT	Maximum output current	Read/Write Word	Linear11
0xDEh	READ_PART_NUMBER	BOM number	Read/Write Block	ASCII
0xDFh	READ_INPUT_TYPE	Input voltage type	Read Word	HEX
0xE0h	WRITE_EVENT_INDEX	Black box No.	Write Byte	DEC
0xE0h	READ_EVENT_LOG	Black box content	Read Block	HEX
0xE1h	WRITE_EVENT_LOG	Writing logs	Write Word	HEX
0xE4h	DCDC_SOFT_VER	DCDC software version	Read Word	HEX
0xE7h	PFC_SOFT_VER	PFC software version	Read Word	HEX
0xEDh	LED_CTRL	LED control	Read/Write Byte	HEX
0xEEh	LOAD_SHARE_SCALE	Coefficient of proportionality for current sharing	Read/Write Byte	DEC
0xF9h	READ_TEMPERATURE_4	Air outlet temperature	Read Word	Linear11
0xFAh	UPDATE_TIME	Time serving	Write Block	TIME
0xFBh	LOAD_PARAM	Load parameters	Read Block	HEX
0xFCh	LOAD_START	Load commands	Read/Write Word	HEX
0xFDh	LOAD_DATA	Data loading	Write Block	HEX

10.3.3 Command Descriptions

PS_CONTROL (0xCEh): PSU control register

Table 10-2 PS_CONTROL (0xCEh)

Byte	Bit No.	Status Bit Name	Meaning
High	F	SF12 (Special Function 12): Fan close	Fan shutdown command. 1: The fan does not work.
	E	SF11 (Special Function 11): N+R Flag	Flag of the N+R power backup function. 0: not supported; 1: supported; write invalidate.
	D	SF10 (Special Function 10): Efficiency Optimized Mode	Reserved bit.
	C	SF9 (Special Function 9): Holdup Optimized Mode	Reserved bit.
	B	SF8 (Special Function 8): Deep Sleep Mode	0b: Disable deep sleep mode 1b: Enable deep sleep mode If SF8 is set to 1, the PSU enters deep sleep mode. In this mode, the PFC, fan, and output of the PSU are disabled when the following conditions are met: 1. The PSU is in parallel mode. 2. EFUSEV is less than 0.8 V. If the backup PSU is powered off (the output voltage is lower than 5.7 V), the PSU automatically exits sleep mode. If SF8 is set to 1, the PSU that works in standalone mode disables the output and restarts. SF8 clearing condition: In SF8 mode, the backup PSU is powered off (the output busbar voltage is lower than 5.7 V).

Byte	Bit No.	Status Bit Name	Meaning
	A	SF7 (Special Function 7): MV6 control	0b: MV6 unshielded mode 1b: MV6 shielded mode • This setting is effective only when PSON12V# is at low level and the PSU enters MV12 mode. • If MV6 mode is shielded and the PSU experiences overtemperature or other failures in MV12 mode, the PSU shuts down the output directly. Clearing condition: The system sets the bit value to 0 or the PSU powers on again (DSP powers on again).
	9	SF6 (Special Function 6): PFC Auto Shut-off	0b: Disable the PFC automatic shutdown control function. 1b: Enable the PFC automatic shutdown control function.
	8	Reserved	Reserved bit.
Low	7	SF4 (Special Function 4): Adjustable V_{out}	0b: Disable output voltage adjustment 1b: Enable output voltage adjustment If SF4 is set to 1, the PSU can adjust the voltage by sending the 21h command, and the current sharing function fails.
	6	Reserved	Reserved bit.
	5	SF2 (Special Function 2): Fan Fault Enabled	0b: Shut down output in case of fan failure 1b: Do not shut down output in case of fan failure • By default, the PSU shuts down if the PSU fan has failed for more than 10s. • If the value of SF2 is 1, the output is not shut down in case of fan failure. The output is shut down if overtemperature protection is triggered.
	4	SF1 (Special Function 1)	Reserved bit.
	3	Reserved	Reserved bit.

Byte	Bit No.	Status Bit Name	Meaning
	2	Interrupt bit	0b: PSU not interrupted 1b: PSU interrupted • An external system cannot set this bit. The value 1 is invalid. • The system can clear this bit. • This bit can be cleared if PSON12V# changes between high level and low level or the PSU powers on again. • After clearing, the PS_interrupt signal of the PSU changes to high level.
	1	Warning Event Mask.	0b: The PSU is not interrupted if a PSU alarm event is generated. 1b: The PSU is interrupted if a PSU alarm event is generated.
	0	Fault Event Mask	0b: The PSU is not interrupted if a PSU shutdown event is generated. 1b: The PSU is interrupted if a PSU shutdown event is generated.

10.4 Online Upgrade

Both the primary and secondary sides of the PSU support online upgrade.

10.5 Black Box Function

The PSU has 440-byte space for storing fault logs. The PSU provides a read channel for external systems by the Read Event Log command.

10.5.1 Runtime Counter

The PSU needs to calculate the total runtime. The total runtime is the sum of the time when the PSU works properly (OPOK# is normal), is presented in the unit of seconds, and occupies four bytes.

10.5.2 Event Log

The PSU maintains a circular event log of the last ten records. Before saving the event log, the PSU shall set the event update flag in the event log to 1. Each event shall start with an event number followed by a 4-byte runtime (measured in seconds). The total runtime must be updated before the log is saved.

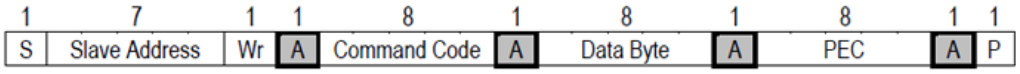
The shutdown event, input voltage, input current, output voltage, output current, temperature, fan speed, maximum input voltage, maximum output current, PS control, and other information will be

stored in the fault record register. The no-output faults caused by insertion or extraction with power on, PSU output command (OPERATION), and CYC_PWR# delivered by the system will not be stored in the PSU fault record. Faults including input power failure, input overvoltage, input undervoltage, output overvoltage, output overcurrent/short-circuit, overtemperature, fan fault, and PSU damage will be stored. If a new fault is the same as the latest record in the event log, this fault will not be stored. That is, two consecutive same faults cannot exist in the fault record.

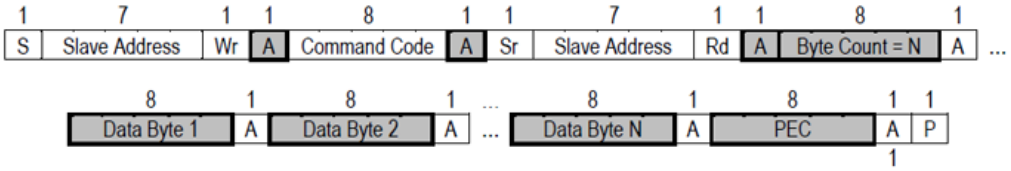
A generated event is saved only when it is different from the last event record. The runtime counter shall be updated every time an event occurs regardless of whether the event is written into the event log. When there are more than 10 events, the 11 event shall overwrite the 1st event, the 12 event shall overwrite the 2nd event, and so on.

10.5.3 Format of Reading Logs

- Write Byte Index(0~10)



- Read Block(N=40)

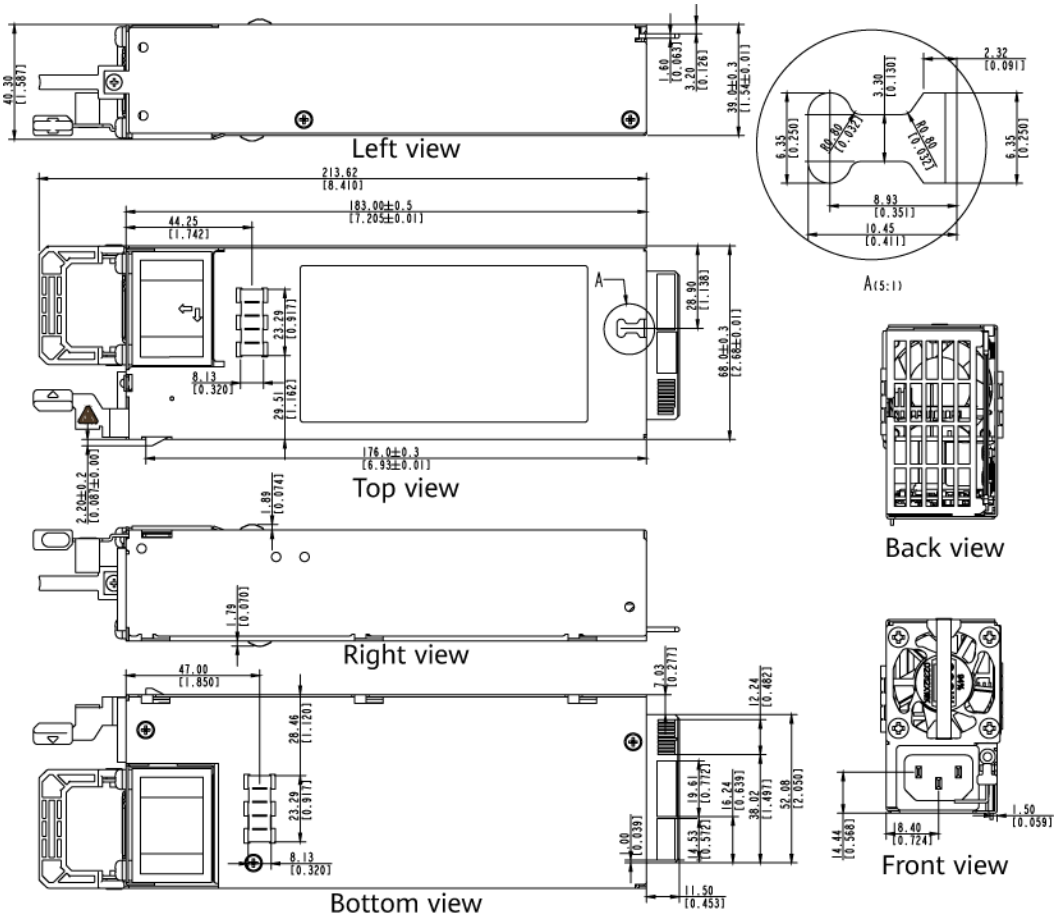


11 Mechanical Overview

11.1 Dimensions

Unit of measurement: mm (in.)

PSU dimensions (D x W x H): 183.0 mm x 68.0 mm x 40.5 mm



11.2 External Ports

Figure 11-1 Output connector (top view)

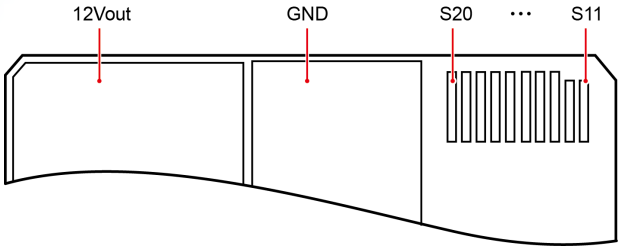


Figure 11-2 Output connector (bottom view)

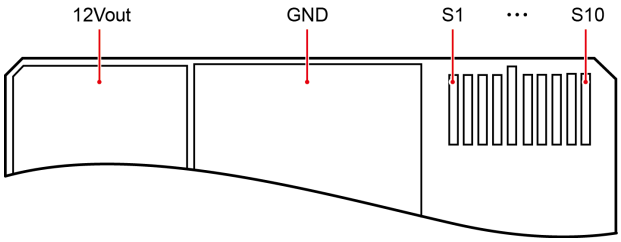


Table 11-1 Output connector pin definitions

Pin	Name	Description
P1–P6, P21–P28	V12	PSU 12 V main output
P7–P20	RTN	PSU output GND
S20	PS_OPOK#	Signal for indicating whether the main output is normal
S19	PS_IPOK#	Signal for indicating whether the input is normal
S18	IPOK Link#	Signal for indicating whether the input of the redundant PSU is normal
S17	SMART_ON#	Signal for waking up cold standby power mode
S16	SHLFBB_SF1	Reserved
S15	INSTALLED54#	Reserved
S14	IP PRESENT#	SV12 control signal
S13	PSON12V#	MV12 remote on/off control signal
S12	INSTALLED#	PSU installation signal

Pin	Name	Description
S11	PRESENT#	PSU presence signal
S10	I-MON#	Current sharing signal
S9	EFUSEV#	System E-Fuse voltage
S8	CYC_PWR#	Power supply cycle power signal
S7	PS_INTR#	PSU alarm interruption signal
S6	SDA	Data cable
S5	I2C Sig GND	I2C signal ground
S4	SCL	Clock cable
S3	ADD2	Address cable 2
S2	ADD1	Address cable 1
S1	ADD0	Address cable 0

11.3 LED Indicator

Indicator	Color	Status	Description
Power status indicator	Orang and green	Steady green	The input and mains MV12 output are normal.
		Blinking green at 1 Hz	1. The input is normal, and the PSU shuts down MV12 output due to the INSTALLED# signal. 2. The input is normal. The PSU enters MV6 mode because the PSON12V# signal is at high level. After the PSU enters MV12 mode due to overcurrent in MV6 mode, the green indicator blinks at 1 Hz. 3. Input overvoltage or undervoltage occurs. 4. The standby PSU is in cold standby mode. 5. The PSU enters deep sleep mode. 6. In low power mode, the PSON12V# and IP PRESENT# signals are at low level and the PSU enters the SV12 mode. After the PSU enters MV12 mode due to overcurrent in SV12 mode, the green indicator blinks at 1 Hz.

Indicator	Color	Status	Description
		Steady orange	The input is normal. There is no output due to overtemperature protection, output overcurrent/short circuit of the PSU in MV12 mode, output overvoltage, short-circuit protection, or component failure (excluding failure of all components).
		Off	No input.
		Blinking green at 4 Hz	Online loading.

NOTE

1. For normal startup, the green indicator should be on and should not blink. For normal power-off, the power indicator should be off and should not be steady red or blinking red.
2. An I2C communication fault is not indicated by the indicator status.
3. When the indicator is controlled by the main control unit, the indicator status depends on the main control unit command.

A Appendix

A.1 EMC Requirements

Parameter	Conditions	Criterion
Conducted emission (CE)	Class A[1], 6 dB	EN 55032
Radiated emission (RE)	Class A[1], 6 dB, 30M–1G	FCC Part15
	Class A[1], 6 dB	EN 55032
Electrostatic discharge (ESD)	Contact: 6 kV, air: 8 kV, criterion B	IEC 61000-4-2
	Contact: 8 kV, air: 15 kV, criterion C	
Electrical fast transient (EFT)	±2 kV, criterion B	IEC 61000-4-4
Conducted susceptibility (CS)	150k–80M, 10 V, criterion A	IEC 61000-4-6
Radiated susceptibility (RS)	80M–6G, 10 V/m, criterion A	IEC 61000-4-3
Surge	AC input surge: Differential mode: ±2.5 kV for L to N (1.2/50 μs, 2 Ω) Common mode: ±2.5 kV for L to PE, N to PE, and L and N to PE (1.2/50 μs, 12 Ω), Criterion B	IEC 61000-4-5
	HVDC input surge: Differential mode: ±2 kV for P to N (1.2/50 μs, 2 Ω) Common mode: ±2 kV for P to PE, N to PE, and P and N to PE (1.2/50 μs, 12 Ω), Criterion B	
Voltage fluctuation and flicker (AC)	Voltage fluctuation and flicker limit of class A products	IEC 61000-3-3

Parameter	Conditions	Criterion
Current harmonics emission (AC)	Harmonic current limit of class A products	IEC 61000-3-2
Power magnetic susceptibility (PMS)	30 A/m, criterion A	IEC 61000-4-8:2001
Dip (AC)	Dip to 0% UT, 100% load, hold-up time: 10 ms	Criterion A (single PSU with full load)
	Dip to 0% UT, 50% load, hold-up time: 20 ms	Criterion A (single PSU with half load)
	Dip to 70% UT, 50% load, hold-up time: 500 ms	Criterion B
	Dip to 0% UT, 50% load, hold-up time: 5000 ms	Criterion C
Dip (HVDC)	Dip to 40% UT: Hold-up time: 1 ms/3 ms/10 ms/30 ms/ 100 ms/300 ms/1000 ms	Criterion B
	Dip to 70% UT: Hold-up time: 1 ms/3 ms/10 ms/30 ms/ 100 ms/300 ms/1000 ms	Criterion B
	Dip to 0% UT: Hold-up time: 1 ms/3 ms/10 ms/30 ms/ 100 ms/300 ms/1000 ms	Criterion B
	Dip to 80% UT: Hold-up time: 100 ms/300 ms/1000 ms/ 3000 ms/10000 ms	Criterion A
	Dip to 120% UT: Hold-up time: 100 ms/300 ms/1000 ms/ 3000 ms/10000 ms	Criterion A

NOTE

1. This is a class A product. In residential areas, this product may cause radio interference. Therefore, users may be required to take appropriate measures.

A.2 Product Safety Testing

A.2.1 Dielectric Strength Testing

Test Item	Minimum Test Voltage	Test Duration	Leakage Current	Expected Result
Input and PE	2500 V DC	1 minute	≤ 10 mA	No breakdown or arcing
	1500 V AC	1 minute	≤ 10 mA	No breakdown or arcing

Test Item	Minimum Test Voltage	Test Duration	Leakage Current	Expected Result
Output and PE	SGND of the 12 V output and the PE are short-circuited inside the PSU.			

NOTE

1. Input to output must meet the reinforced insulation requirements after the output ground is disconnected from the PE.
2. Input to output: 4242 V DC, 1 minute, 10 mA; complies with IEC 62368-1.

A.2.2 Ground Continuity Testing

Test Item	Maximum Test Voltage	Test Current	Maximum Resistance	Test Duration
PE input and shell	12 V	25 A	0.1 ohm	Until the readings are stable.

NOTE

This test item is applicable only to power supply devices with metal shells or L-shaped supports that are connected to the PE.

A.3 Reliability

Parameter	Min.	Typ.	Max.	Unit	Notes & Conditions
Mean time between failures (MTBF)	-	500,000	-	Hours	Telcordia SR332; V_{in} = 230 V AC/240 V DC; Rate load; T_A = 25°C

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